block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

an means-basis ECC block pipeline processing notification sub means

5   for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said ECC-block-basis buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

10   a means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said

15   error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting

20   means; and

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said

25   DMA transfer instruction sub means in said system control means

recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the

5   code words which are to be processed therein.

17.   The error correction device of claim 9, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising

10   a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are

15   subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code

20   word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

an means-basis ECC block pipeline processing notification sub means

25   for transmitting ECC blocks which have been subjected to error correction

downstream; for storing ECC blocks to be processed next to said ECC-block-basis buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

5 a means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said

10 error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting

15 means; and

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said

20 DMA transfer instruction sub means in said system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the

25 code words which are to be processed therein.